

**REMARKS**

Claims 1-20 are pending in this application. In the Office Action, claims 1-7 are rejected over prior art. Claims 18 and 19 are amended. Reconsideration of the rejection is respectfully requested.

Claims 18 and 19 are amended to correct typographical errors.

**ELECTION/RESTRICTIONS**

Applicants again respectfully submit that the Examiner has made an improper restriction. Assuming *arguendo* the Examiner has made a proper restriction with regards to new claim 15-19, the Examiner restriction requirement with regards to claims 1-7 and claim 8-14 and 20 is improper.

The Examiner states that "amendments to independent claims 1 and 8 (in view of the office action dated 06/16/2005), and new independent claim 15 are patentably distinct for the same reasons as mentioned in the last office action (dated 09/26/2005)." However, the Examiner has failed to respond how any serious burden has been placed on the Examiner when the Examiner has already searched and examined claims 1-14.

Applicants may traverse the Examiner's restriction requirement, if Applicants can show that the application can be examined without any serious burden on the Examiner. See MPEP 803. Applicants submit that any amendments made to independent claims 1 and 8 by the Amendment filed on 09/07/2005, did not change the nature, i.e., class and subclass, of independent claims 1 and 8.

Accordingly, the Examiner had already searched and examined independent claims 1 and 8; Applicants amendment to claims 1 and 8 did not change the nature of these claims. Therefore, no serious burden has been placed on the Examiner to examine at least claims 1-14 as a whole.

Applicants respectfully request the Examiner to withdraw the restriction requirement for at least Groups I and III.

**CLAIM REJECTION UNDER 35 U.S.C. §102**

Claims 1 and 5 rejected under 35 U.S.C. § 102(b), as being anticipated by Jeng et al. (U.S. Patent 6,097,199). The rejection is respectfully traversed.

Applicants submit that claim 1 provides “a device under test (DUT) board connectable between the mother board and the semiconductor device chip to be tested”. On the other hand, Jeng et al. discloses “a test socket 202” between a universal decoder test board (UDTB) 204 and a semiconductor device chip to be tested. interfaces with a tester interface board 206. A tester interface board and a test head are completely different structures.

First, Applicants submit that claim 1 recites in part that “a mother board [is] electrically compatible with each of respective test heads of [] different testers[.]” In other words, the mother board is compatible with many different types of test heads.

On the other hand, Jeng et al. discloses that “a universal decoder test board (UDTB) 204 interfaces with a tester interface board 206. A tester interface board and a test head are completely different structures.

“A universal decoder test board (UDTB) 204 interfaces with a tester interface board 206 which is specifically designed to interface with a tester for a particular manufacturer’s hardware platform (not shown).” (Emphasis added.) Column 3, lines 48-52.

In other words, the tester interface board 206 is compatible with different testers, not that the UDTB 204 (alleged by the Examiner as the mother board) is compatible with different testers (as recited in claim 1). See also Column 2, lines 19-23, and column 4, lines 56-58.

The Examiner also alleges Jeng et al. discloses that the mother board 204 (UDTB) includes connectors 202, and the connectors 202 are located at a central portion of the mother

204 and adapted to transmit electrical signals. The Examiner further alleges that a socket 202 is equivalent to a device under test (DUT), the socket 202, i.e., DUT, and adapted to receive the electrical signals from the mother board.

As readily apparent from the above paragraph, a socket 202 of Jeng et al. **cannot** be both connectors and a device under test (DUT) at the same time physically or functionally. The socket 202 cannot at the same time send electrical signals and then receive said electrical signals. In addition, Jeng et al. specifically discloses that UDTB 310 functions as the conventional DUT. Column 4, lines 66-67.

Applicants again respectfully submit that Jeng et al. fails to teach or suggest: (1) a mother board electrically compatible with each of respective test heads of different testers; (2) the mother board including connectors adapted to transmit electrical signals; and (3) a DUT adapted to receive said electrical signals.

For at least the reasons given above, claim 1 is patentable over the Examiner's cited reference. In addition, claim 5 dependent on claim 1 is also patentable for the same reasons given with respect to the patentability of claim 1.

#### **CLAIM REJECTION UNDER 35 U.S.C. §103**

Claims 2-4 and 6-7 are rejected under 35 U.S.C. §103(a) as being unpatentable over Jeng et al. in view of Applicants admitted prior art. This rejection is also respectfully traversed.

Applicants respectfully submit that claims 2-4 and 6-7, which directly or indirectly depend on claim 1, are also patentable for the same reasons given with respect to the patentability of claim 1. Applicants also submit that the APA does not cure the deficiencies of Jeng et al.

**CONCLUSION**

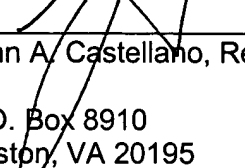
In view of the above remarks, reconsideration of the rejections and allowance of claims 1-20 are respectfully requested.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below. If the Examiner believes that a personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (703) 668-8000.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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By   
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